Computer organization and Architecture (COA)

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~~Number~~ ~~Deci~~

→ Basic functional Units of a Computer

Input Unit → Takes input from user

Memory Unit → Stores data, instructions, and results (RAM, ROM, Hard Drive)

Control Unit → Directs the flow of data and controls operations of other units

Arithmetic Logic Unit (ALU) → Performs all arithmetic and logical operations.

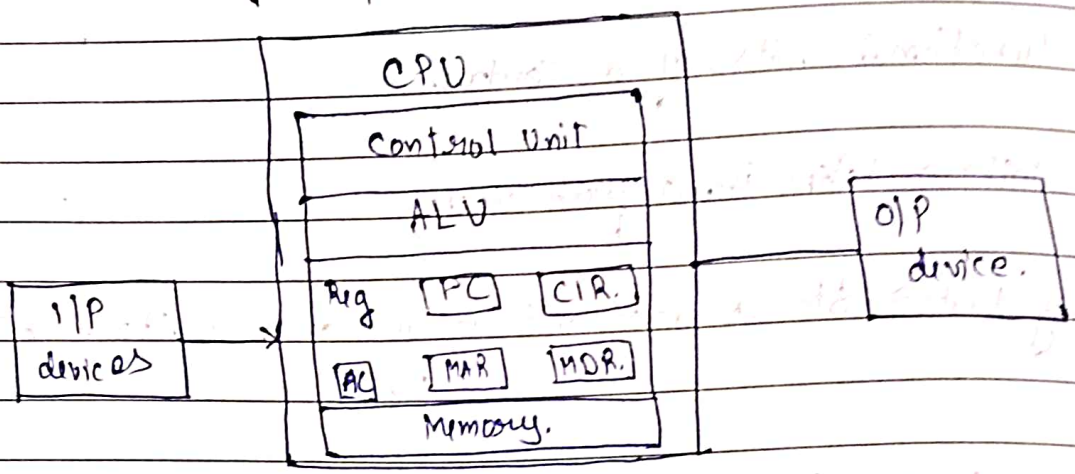
Output Unit → Displays the result (monitor, printer, etc)

Central Processing Unit → The 'brain' of the computer - consists of CU + ALU

→ Generations of Computers

Gen	Time Period	Technology used	Features.
1st Gen	1940-1956	Vaccum Tubes	Very large, slow, machine language
2nd Gen	1956-1963	Transistors	Smaller, faster, used assembly langua
3rd Gen	1964-1971	Integrated Circuits	High-level programming languages used
4th Gen	1971-Present	Microprocessor	Personal comp, graphical user interfaces
5th Gen	Present & Beyond	AI, Robotics, Quantum	Smart computers, voice recognition, robotics.

Architecture of Computers



PC - Program Counter
CIR - Current Instructions Resistar
AC - Accumulatar
MAR - Memory Address ~~Resistor~~ Registar
MDR - Memory Data Resistar

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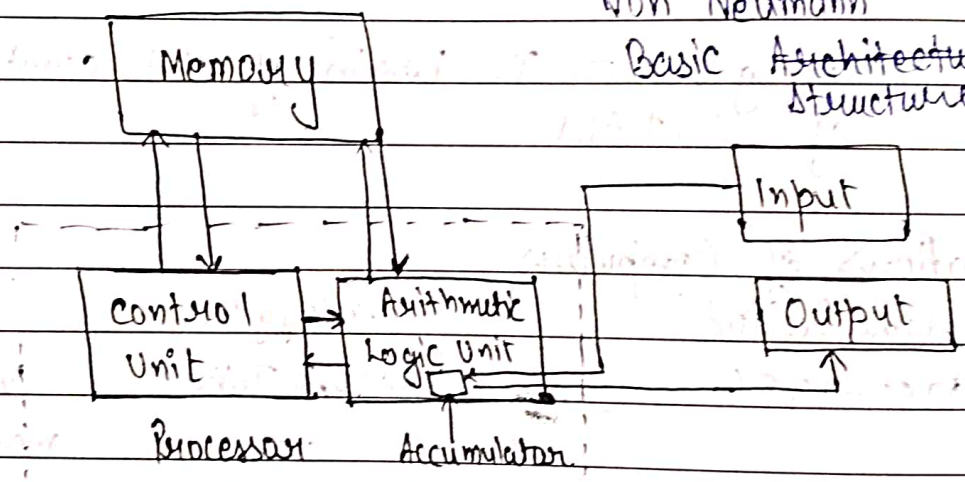
Von Neumann
Basic ~~Architecture~~ Structure.



This architecture is based on the stored program computer concept. i.e. where the instructions data and program data are stored in the same memory.

① CPU (Central Processing Unit) - It is responsible for executing the instructions of the computer program.

② Registers - Data needs to be stored in registers before it is processed, they are the high speed storage area.

MAR - Memory Address Register
It holds the memory location of the data that needs to be accessed.

MDR - Memory Data Register
It holds the data i.e being transferred to or from memory.

AC - Accumulator - It is where intermediate arithmetic and logical results are stored.

PC - Program Counter - It contains the address of the next instructor to be executed.

CIR - Current Instruction Register - It contains the current register during processing.

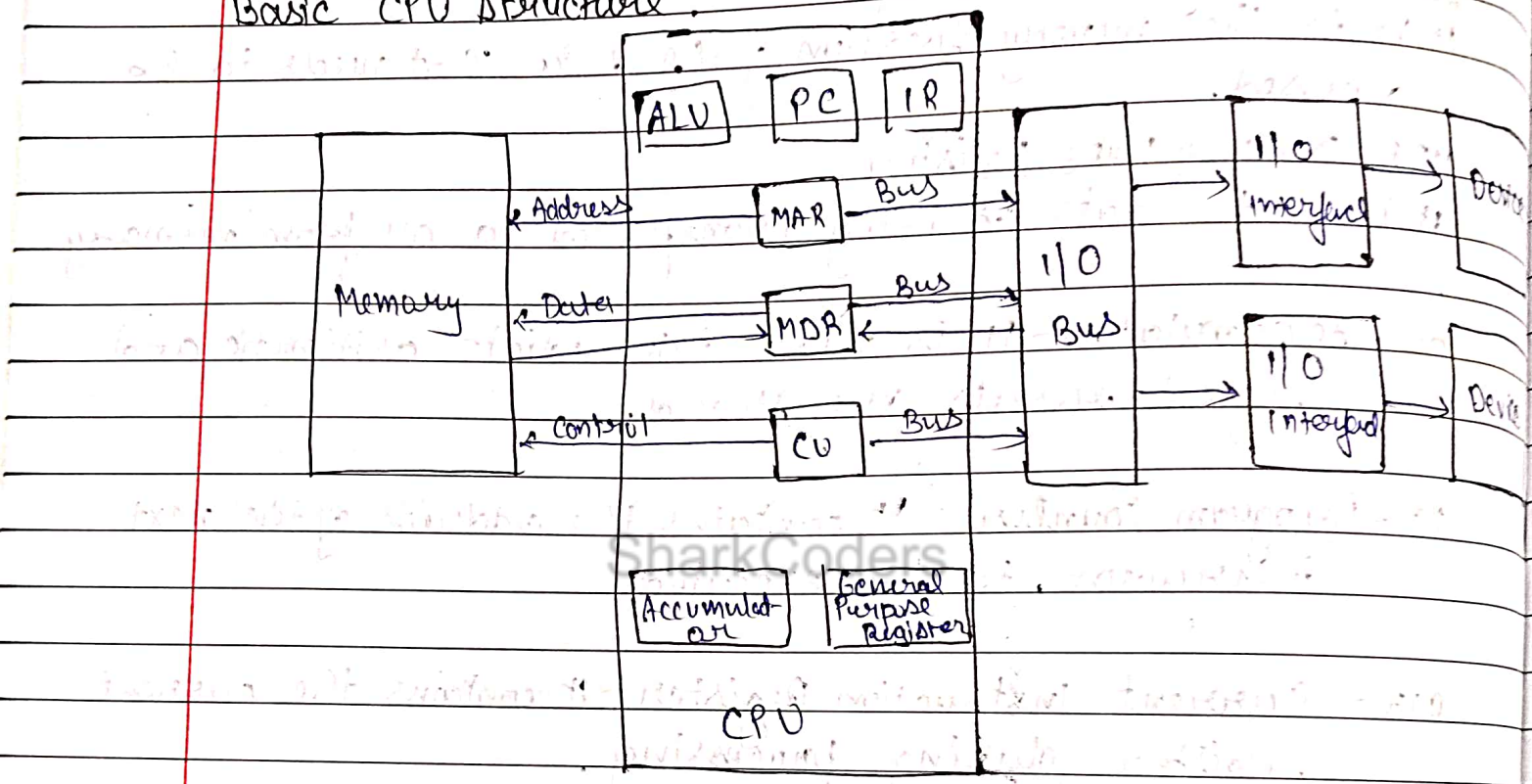
③ ALU - Arithmetic Logical Unit.
arithmetic (+, -, ×, ÷)
logical (AND, OR, NOT, etc).

④ CU - Control Unit - It tells how to respond to the program instruction which it has just read and interpreted from the memory unit.

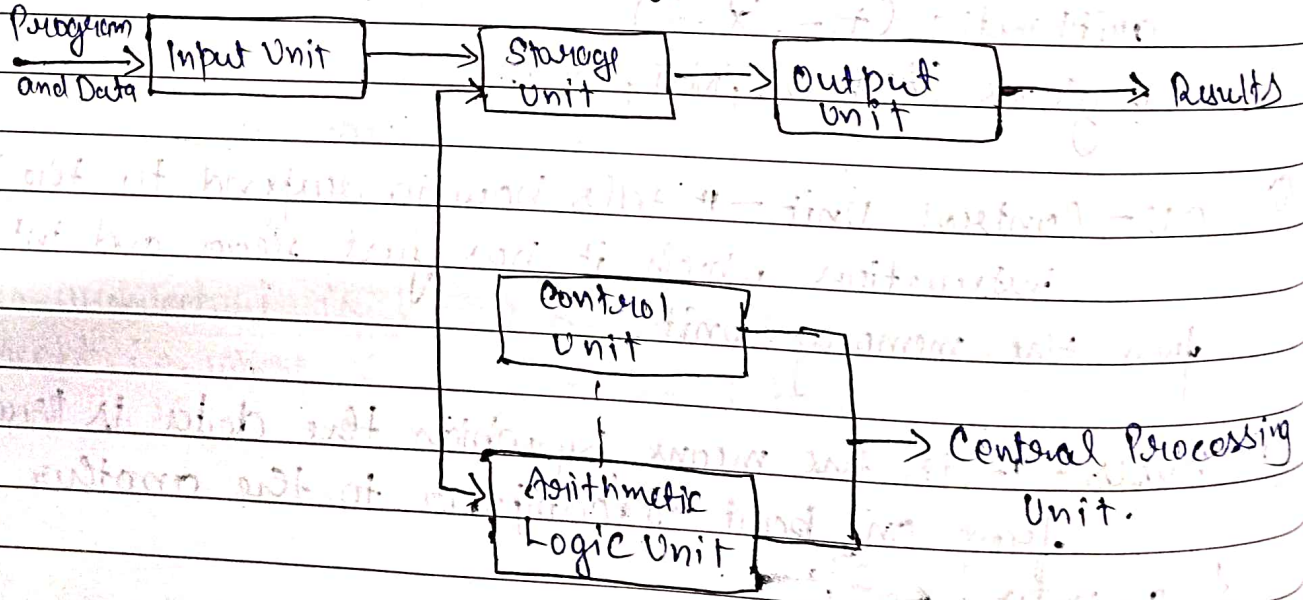
⑤ Buses - It is the means by which the data is transmitted from one part of computer to the another part of computer.

⑥ Memory Unit - It consists of RAM, sometime referred to as primary or main memory unlike a hard drive i.e. secondary memory, this memory is fast and is also directly accessible by CPU.

Basic CPU structure.



Functional units of Computer System.



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Bus Structure:
Bus architecture
Bus structure in computer architecture is a shared set of electrical pathways that connect components such as the CPU, memory, and I/O devices, enabling them to transfer data, addresses, and control signals.

Key point about bus structure:
- The bus acts as a communication system within the computer, allowing for efficient exchange of information among hardware components.
- Most computer systems use a system bus that consists of three main types of buses:

- Data Bus: Transfers actual data b/w components; it is typically bidirectional, meaning data can flow both ways. The width of the data bus determines how much data can be transferred at once.
- Address Bus: Carries memory addresses specifying where data is to be read or written. It is unidirectional and its width determines the amount of addressable memory.
- Control Bus: Transmits control signals (such as read/write, interrupt, timing signals) to coordinate operation b/w CPU and other devices.

- Bus architecture are classified into types such as:
- Single Bus Structure: All components share one common bus, making it simple and cost-effective but with reduced performance and scalability due to possible bottlenecks.

- Multi-Bus (Double Bus) structure: Multiple buses separate data and instructions transfers, improving performance and scalability but increasing complexity and cost.

Feature	Single Bus Structure	Double Bus Structure
Number of Buses	One shared bus	Two independent buses (data & instruction)
Cost	Low	Higher
Performance	lower (possible bottlenecks)	Higher

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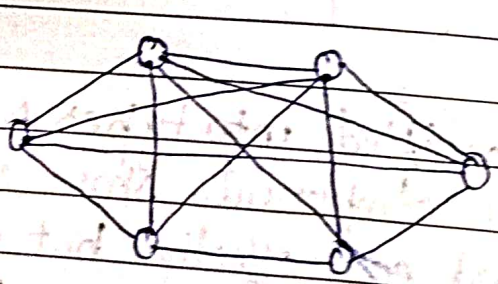
Interconnection networks.

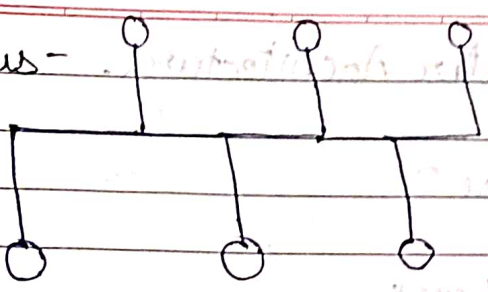
Nodes –

- Static
  - Ring Bus
  - Shared Bus
  - Tree
  - Completely Connected networks.
- Dynamic
  - Crossbar Switch Connections
  - Multistage Interconnect network
  - Single Stage Interconnect network

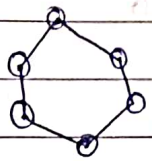
① Completely connected networks –



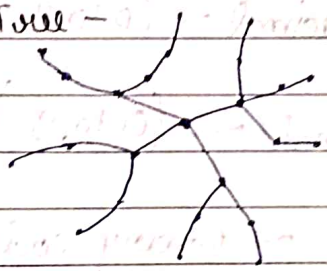
(2) Shared Bus -



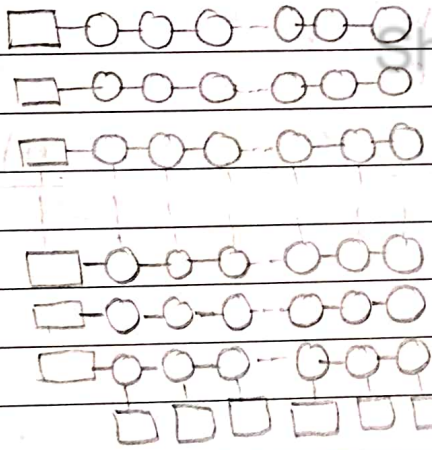
(3) Ring

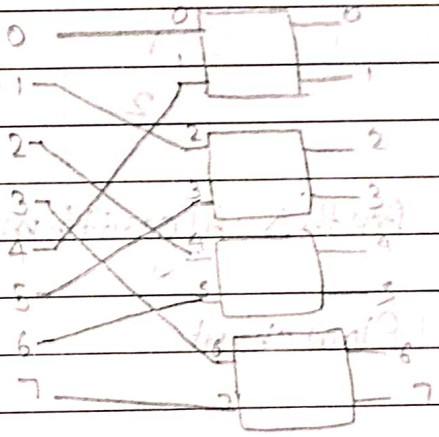


(4) Tree -

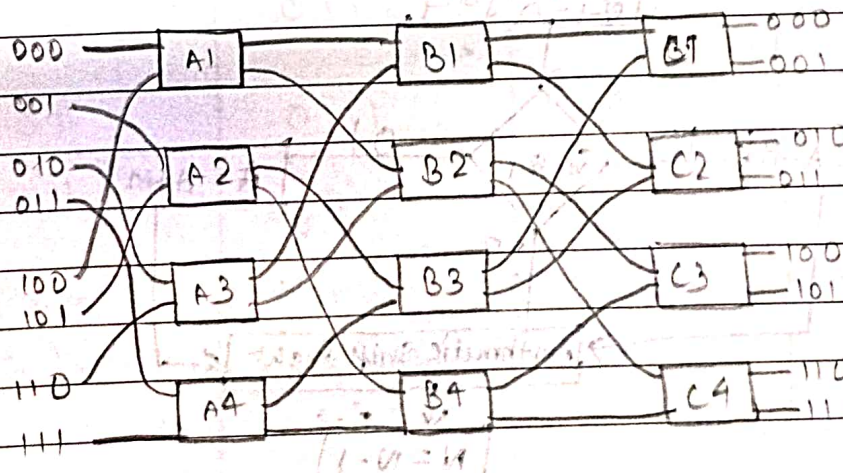


(1) Crossbar Switch connections 2. Single Stage Interconnect Network





3. Multistage Interconnect Network



Data Types & Computer Architecture.

① Binary - (0 & 1) & base 2

② Octal - (0 to 7) base 8

③ Hexadecimal - (0 to 9 & A to F) base 16

④ Decimal - (0 to 9) base 10.

⑤ BCD - Binary coded Decimal.

~~Binary~~ Decimal	~~Bin~~ BCD
0	0000
1	0001
2	0010

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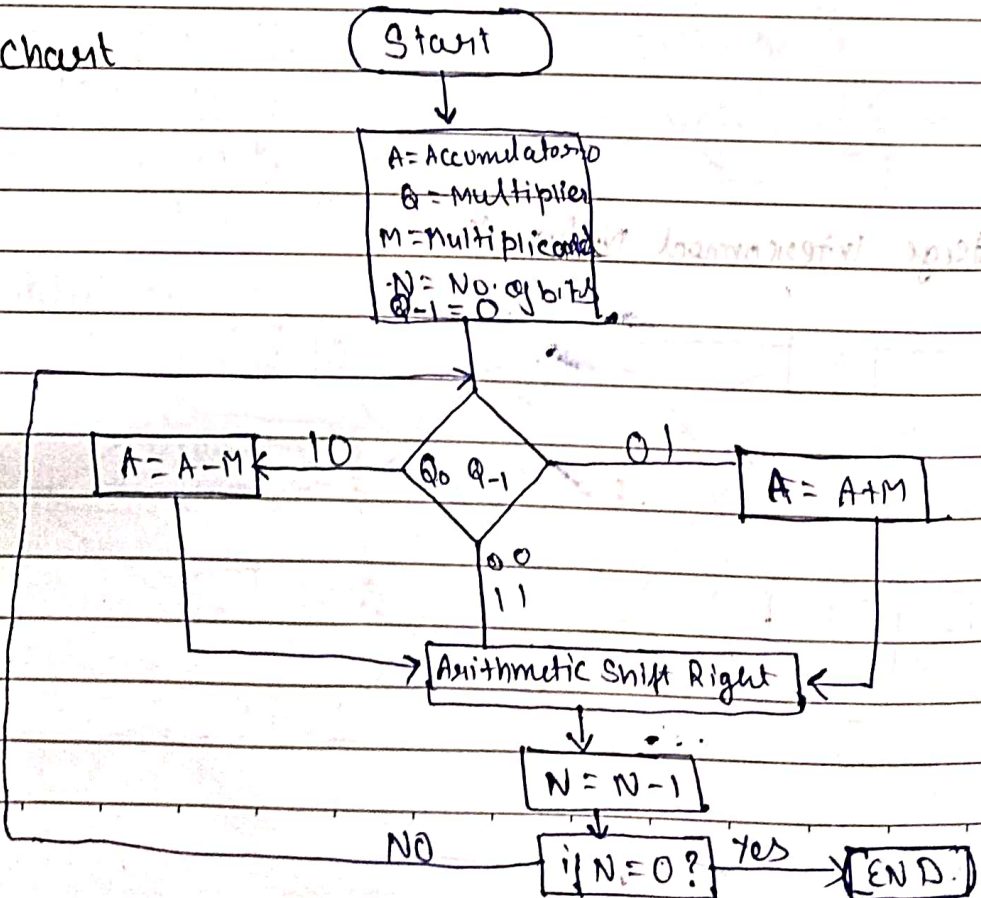
★★ Booth's Algorithm

- Flowchart



• 7 × 3

	A	Q ($Q_3 Q_2 Q_1 Q_0$)	Q_{-1}	Operation	M = 7 = 0111 Q = 3 = 0011 N = 4
1)	0000	0011	0	A = A − M A = 0000 + 1001 1001	Q_0 Q_{-1} 1 0
	1001	0011	0	ASR.	M = 1's → 1000 + 1 2's com 1001 − M =
	1100	1001	1	ASR.	Q_0 Q_{-1} 1 0
2)			1		1 1
3)	1110	0100	1	A = A + M A = 1110 0111 10101 A	0 1
	0101	0100	0		0 0
4)	0010	0010	0		
			0		

00010101 = 21

• 3 × 7

	A	Q	Q_{-1}	Operation	M = 3 = 0011 Q = 7 = 0111 N = 4
1)	0000	0111	0	A = A − M 0000 + 1101 1101	M = 1's = 1100 + 1 2's 1101 − M = 1101
	1101	0111	0	ASR	Q_0 Q_{-1} 1 0
			1		1 1
2)	1110	0011	1	ASR	1 1
			1		0 1
3)	1111	0001	1	ASR.	
			1		

4)

1111	0010	1	A = A+M.
			1111
			0011
0000	1010	1	10000
0000	0101	0	
0001	0101	0	

00010101 = 21

Solve 2 * 5

M = 2 = 0010 → 1101 N = 4

Q = 5 = 0101 +1

1110 = -M

	A	Q	Q-1	operation	Q0 Q-1
1)	0000	0101	0	A = A-M.	1 0
	1110	0101	0	0000	0 1
				-1110	1 0
				1110	0 1
				ASR.	
2)	1111	0010	1	A = A+M	
				1111	
	0001	0010	1	0010	
				10001	
3)	0000	1001	0	A = A-M	
				0000	
	1110	1001	0	1110	
				1110	
				ASR.	
4)	1111	0100	1	A = A+M	
				1111	
				+0010	
	0001	0100	1	10001	
	0000	1010	0		10 → 00001010

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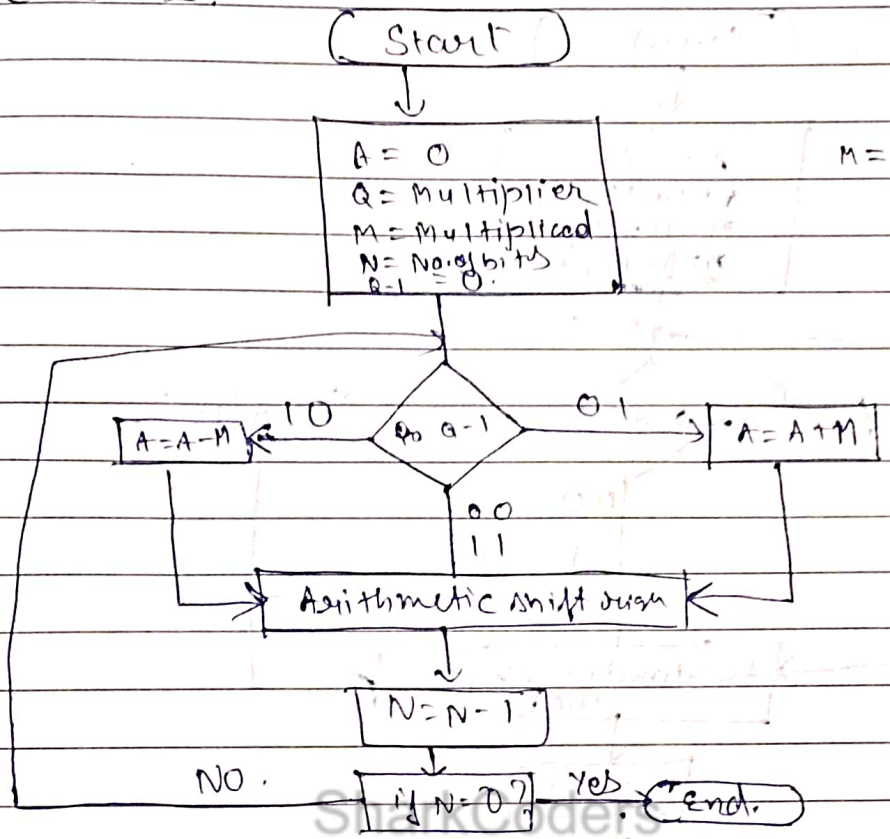
- Solve 5 * 2.



M = 5 = 0101

Q = 2 = 0010

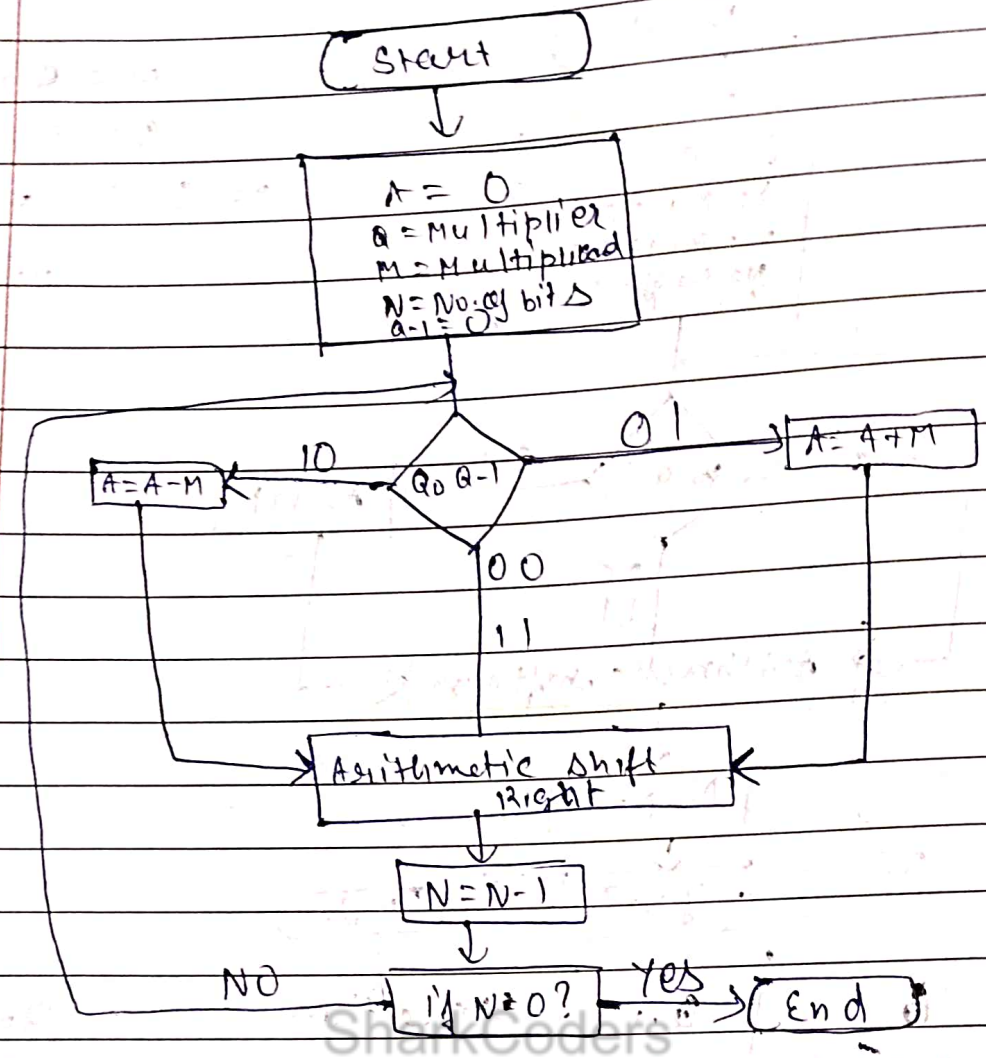
M = 0101 = 1010

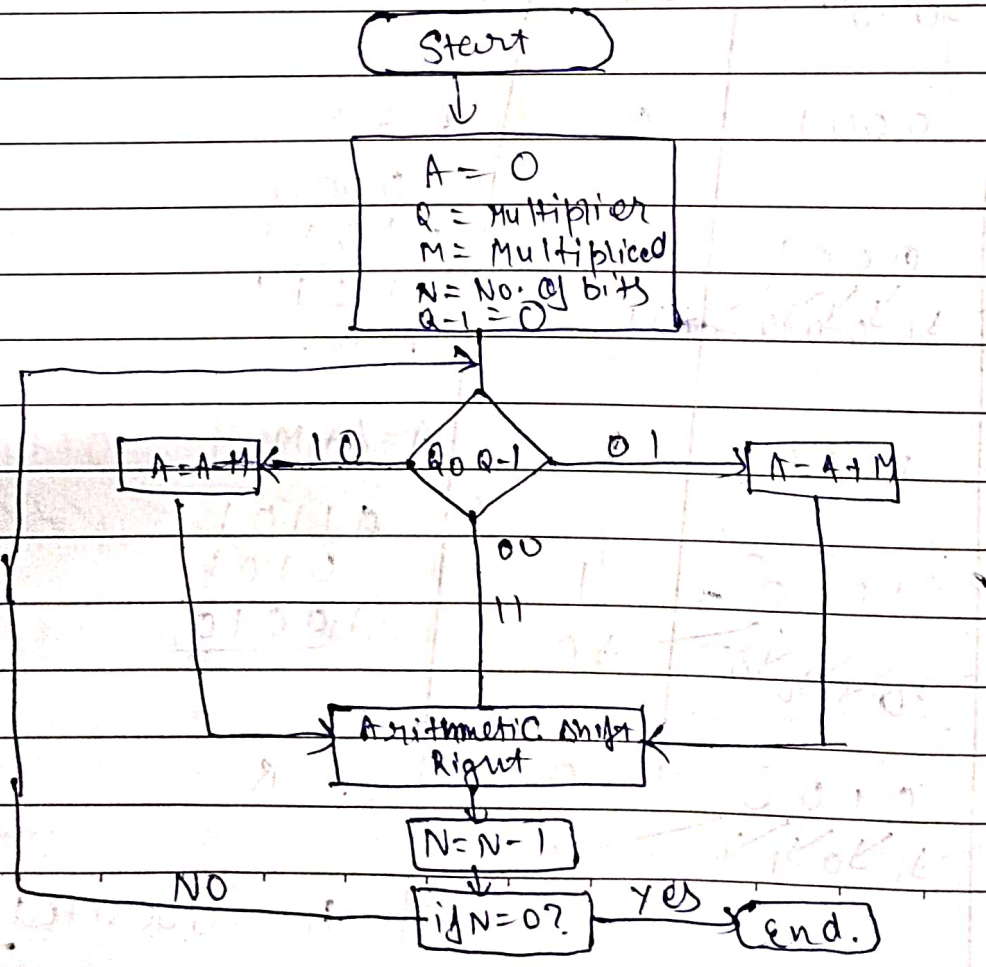
+1

-M = 1011

	A	Q	Q-1	operation.	Q0 Q-1
1)	0000	0010	0	ASR.	0 0
	↓ 0000	0001	0		1 0
					0 1
2)	0000	0001	0	A = A - M	0 0
				0000	
				+ 1011	
	1011	0001	0	1011	
	↓ 1101	1000	1	ASR.	
3)	1101	1000	1	A = A + M	
				1101	
				0101	
	0010	1000	1	10010	
	↓ 0001	0100	0		
4)	0001	0100	0	ASR	
	↓ 0000	1010	0		

10 → 00001010





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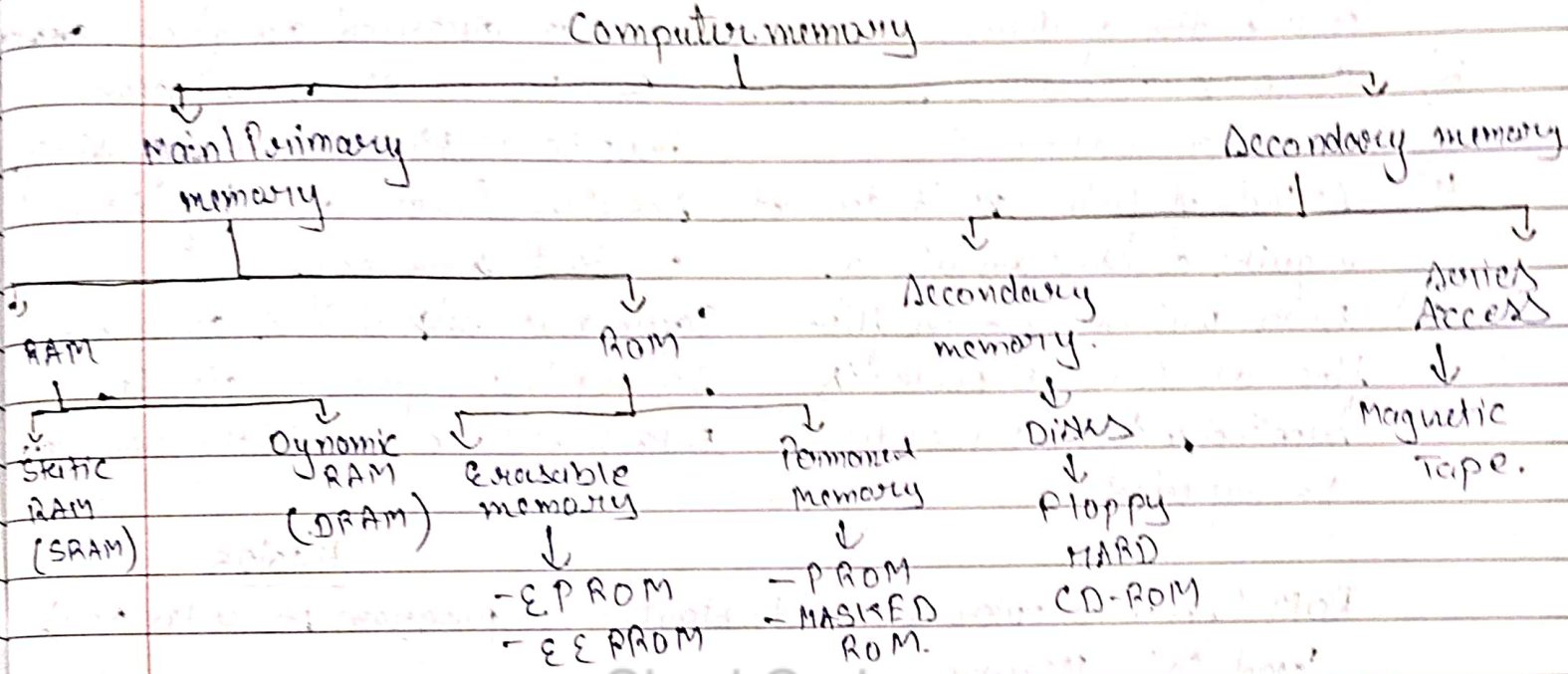
Unit. 2

Memory System



Primary Memory	Secondary Memory
1) ~~Group~~ Lookwise size is small	Lookwise size is bigger
2) Storage capacity is large and fast accessing.	Larger capacity but slower than primary memory
3) It stores the program along with the data which are currently being executed.	It is a permanent storage type used to store data and programs that are not frequently used.
4) It also stores necessary programs of system software	It also acts as an overflow memory when the capacity of primary memory is exceeded.

- RAM is a volatile memory (looses data when power down).
- ROM is a non volatile memory (keeps data even after power cut down).

Static RAM	Dynamic RAM
1) Faster and more expensive	Slower and more affordable
2) Flip-flops are used to stores each bit of data.	stores each bit of data as an electrical charge on a cell
3) Complex circuitary so more power consumption.	Less power consumption inspite of the need of refreshing
4) Speed is faster as it does not require constant refreshing.	Speed is slower as it requires constant refreshing.
5) Data will be held in flip-flop as long as power is supplied so does not need to be refreshed.	Capacitors leak charge over time so requires refreshing circuit. Data must be constantly rewritten

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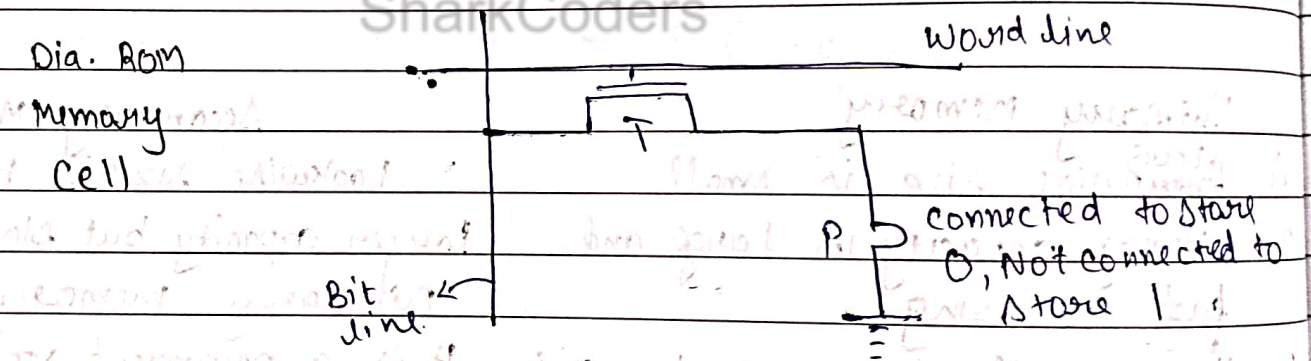
ROM (when computer wants to start that program stores in ROM)
Read Only Memory



- To drive the bit which is in memory cell you have to activate word line.

Types of ROM.

1) PROM (Programmable Read only memory)
- Programmed by the user
- Cannot erase once stored (Permanent)
- Data and instruction cannot be changed.

2) EPROM: Erasable Programmable Read only memory
- It can be reprogram.
- You cannot erase some portion, You have to erase all data

- To erase data expose it to UV (Ultraviolent) lenght.
- To re-program erase all the previous data.

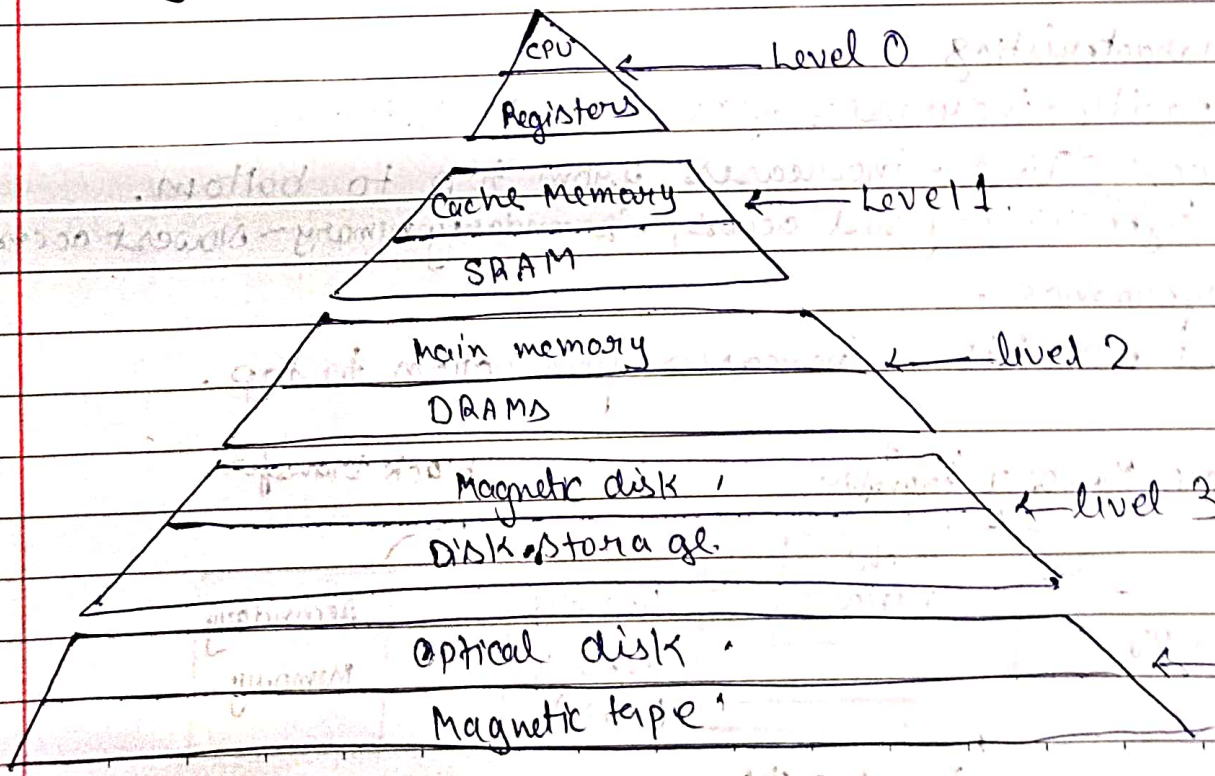
3) EEPROM – (Electrically Erasable programmable Readonly memory)

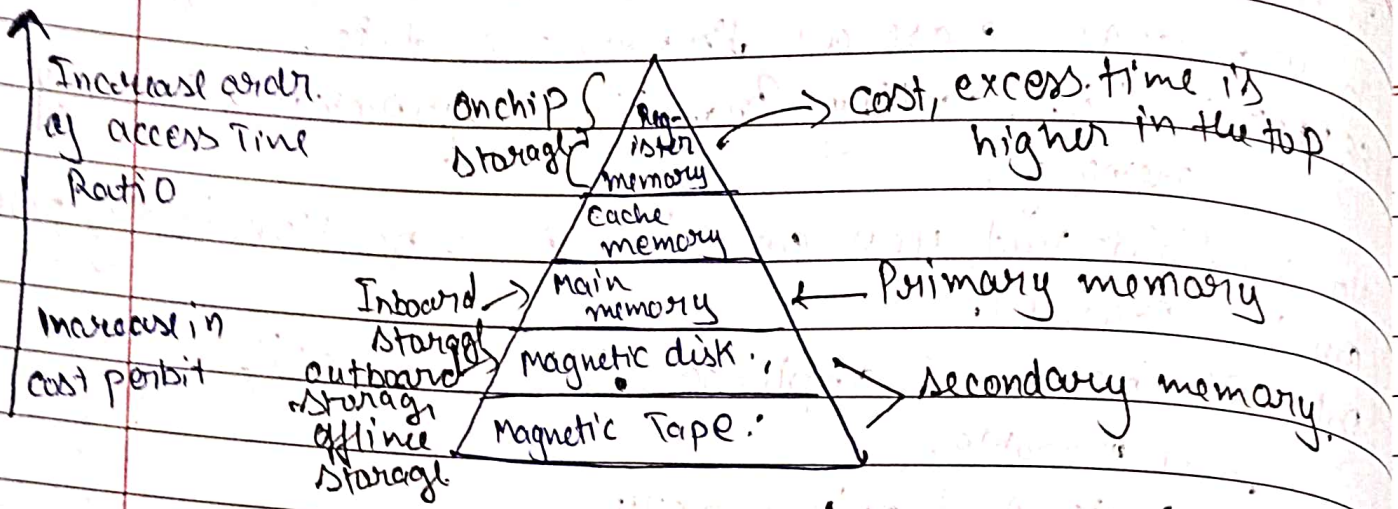
- No UV light need, you can erase some portion (only portion can be erased).
- Data can be erase applying electrical field.

→ not erasable.

4) MROM – Mask Read only memory
- It cannot be change
- It is low cost and highly reliable.
- ROM chip where data is permanently programme during the manufactuering process using a physical mask and cannot be change later.
- Fast Read speed.
- Used for fixed and critical data application such as microcontrollers and embedded system. etc.

– Memory Hierarchy :-





Types of Memory Hierarchy

Memory Hierarchy is divided into two parts:
1) External & 2) Internal memory.

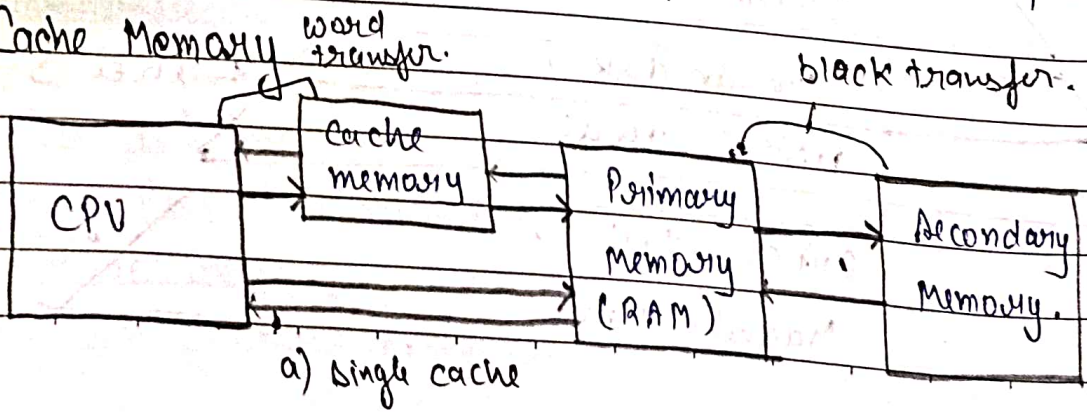
External It comprises of magnetic disk, optical disk & magnetic tape. These devices are accessible by the processor via Input/Output module.

Internal It comprises of main memory, cache memory & CPU registers. These devices are directly accessible by the processor.

Characteristics

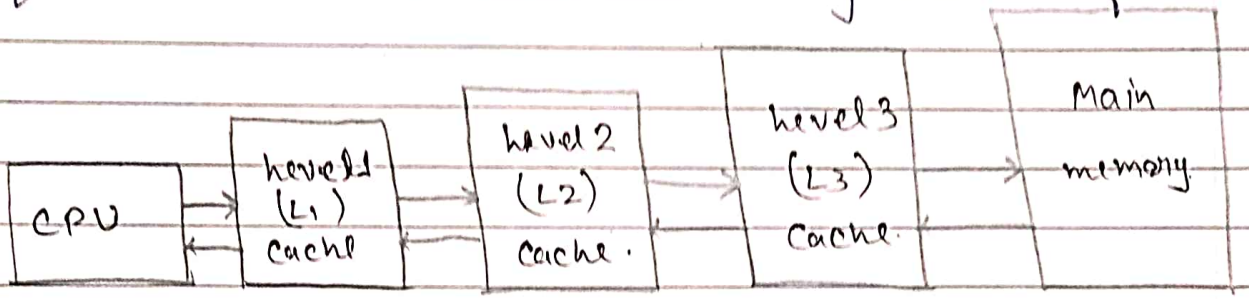
1) Capacity - increases from top to bottom.
2) Access Time - increases from top to bottom.
   Register memory - fastest access, : Secondary memory - slowest access.
3) Performance.
4) Cost per bit - increases from bottom to top.

Cache Memory



a) Single cache

Small in size., high speed memory located b/w. CPU and main memory. (RAM). It acts as a buffer to bridge the speed. gap b/w the fast CPU and slower RAM, improving overall system performance. by providing the CPU with quick access to the most commonly needed information.



b) 3-level cache. organization.